Open Floating Point Unit

The Free IP Cores Projects
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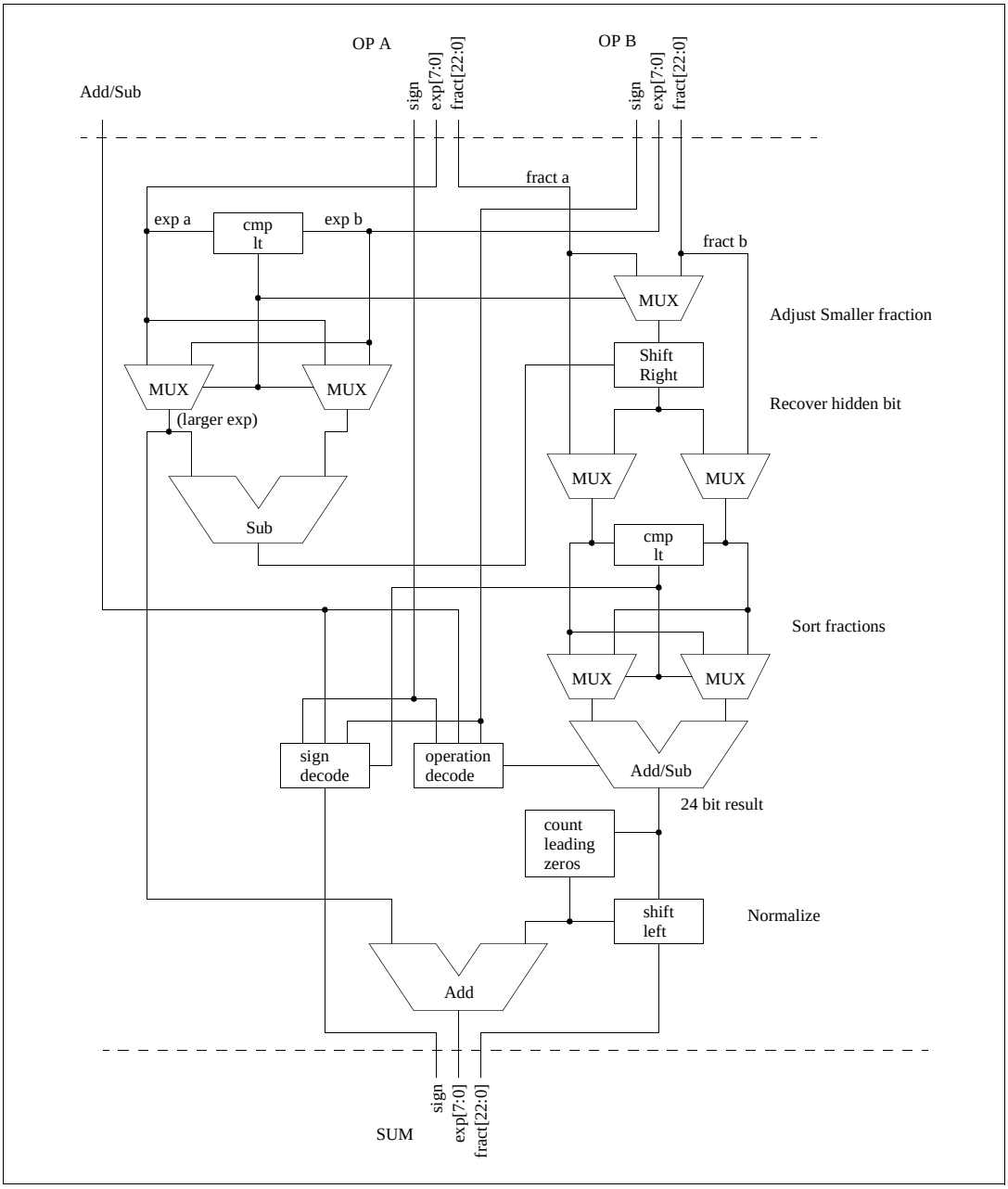
Summary:
This documents describes various building blocks for a single precision floating point unit. The minimum targeted set should include Add, Sub, Mul and Div operations. The blocks will be first presented as stand alone units, later integrated in to a single FPU block.

1. Change Log

7/14/2000 RU
- Added FMUL
- Removed Exception block (generates INF and NAN exceptions). Exceptions will be handled on a global level later on ...

2. FASU - A Floating Point Add/Subtract Unit

The FASU is a single precision floating point add/subtract unit.It is fully IEEE 754 compliant. Below diagram illustrates the internal of this implementation (pipeline not shown).

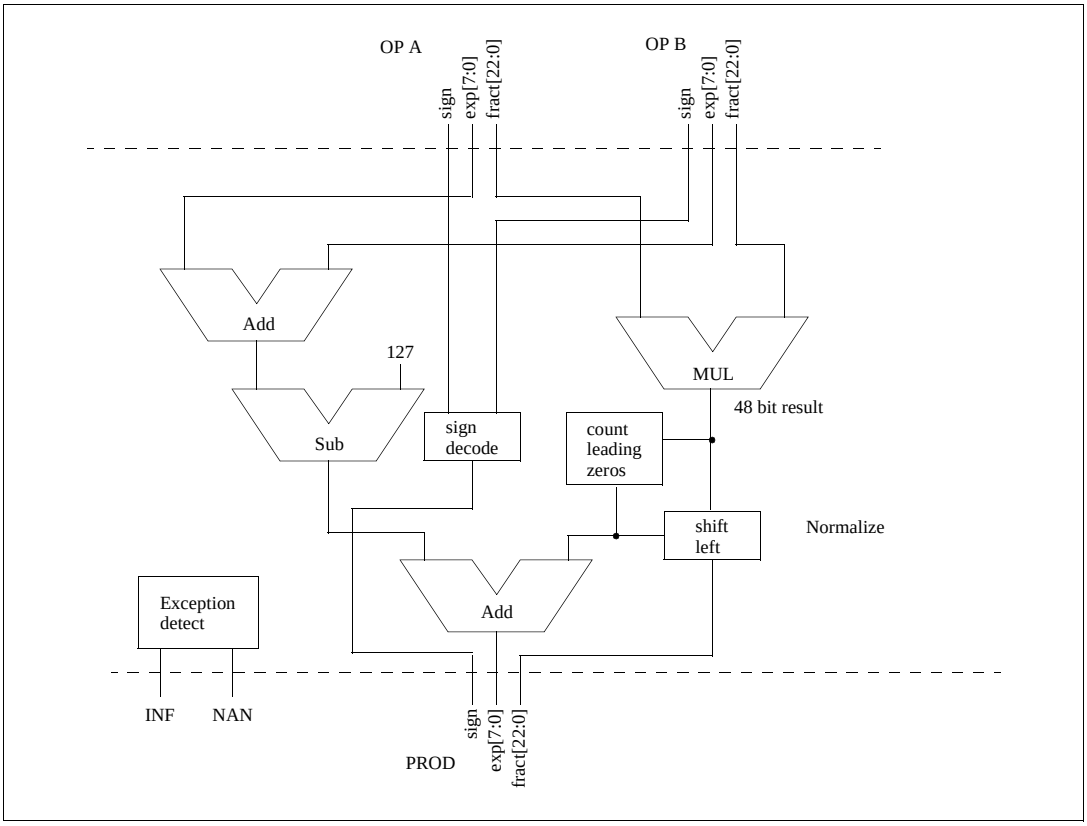


Known incompatibilities/shortcomings:

- INF and NAN might not be properly represented on the output, this will be fixed in an upper level
- Results are truncated, this should be changed to proper rounding, even though truncating is OK per IEEE

3. FMUL - A Floating Point Multiply Unit

The FMUL is a single precision floating point multiply unit.It is fully IEEE 754 compliant. Below diagram illustrates the internal of this implementation (pipeline not shown).



Known incompatibilities/shortcomings:

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4. FDIV - A Floating Point Divide Unit