Information in this document is provided in connection with Intel products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

The

28F016S3

28F008S3

28F004S3

2.0 PRINCIPLES OF OPERATION

The 3 Volt FlashFile memories include an on-chip WSM to manage block erase, program, and lock-bit configuration functions. It allows for: 100% TTL-level control inputs, fixed power supplies during block erasure, program, and lock-bit configuration, and minimal processor overhead with RAM-like interface timings.

After initial device power-up or return from deep

When the block erase is complete, status register bit SR.5 should be checked. If a block erase error is detected, the status register should be cleared before system software attempts corrective actions. The CUI remains in read status register mode until a new command is issued.

Table 6. Status Register Definition

WSMS	ESS	ECLBS	PSLBS	VPPS	PSS	DPS	R

6.0 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings*

Temperature under Bias.....–10 °C to +80 °C

Storage Temperature .....–65 °C to +125 °C

Voltage On Any Pin
(except V_{PP}, and RP#).....–2.0 V to +7.0 V(2)

V_{PP} Voltage.....–2.0 V to +14.0 V(1,2)

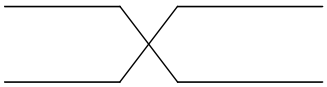
RP# Voltage..... –2.0 V to +14.0 V(1,2,4)

Output Short Circuit Current..... 100 mA(3)

6.4 DC Characteristics—Commercial Temperature

	2.7 V V_{CC}	3.3 V V_{CC}	Test

PRELIMINARY



E