Contents

WB Write Fifo read enable is active, read address from ***wbw_fifo_control.v*** is applied to RAM interface, to provide next data at its data outputs. Address/data output from WB Write Fifo is connected to ***pci_master32_sm_if.v***. When data marked as last (determined

stored in WB Read Fifo (determined by a state of read counter), external Target Disconnects or Master Abort or Target Abort is signaled. In later two cases, data entry will still be written to WB Read Fifo marked as error on WB Read Fifo control bus

- **disconect_wo_data_out**

Configuration read from Configuration space starts, when PCI signal IDSEL is active and CONF READ command is performed (all CONF READ commands are single reads and DWORD aligned).

Logic in PCI target state machine just set the current address to Configuration

- **wb_img_ctrl*** (bits 2-0 of W_IMG_CTRL* register): connected to ***decoder.v***

- PCI_FIFO_RAM_ADDR_LENGTH – must be equal to address length of instantiated RAM in **pci_tpram.v**.
- instantiated RAM in

all PCI devices are connected correctly in the testbench with PCI Master configuration cycles.

"WB ERROR CONTROL AND STATUS REGISTER VALUE CHECK AFTER CLEARING ERROR STATUS"

"INTERRUPT REQUEST ASSERTION AFTER ERROR REPORTING TRIGGER"

"PCI DEVICE STATUS REGISTER VALUE CHECK AFTER TARGET ABORTED MEMORY WRITE"

"INTERRUPT STATUS REGISTER VALUE CHECK AFTER CLEARING STATUS BITS"

"WB ERROR STATUS REGISTER VALUE CHECK AFTER CLEARING STATUS BIT"

"WB ERROR STATUS REGISTER VALUE CHECK AFTER READ TERMINATED WITH TARGET ABORT"

"PCI DEVICE STATUS REGISTER VALUE CHECK AFTER READ TERMINATED WITH TARGET ABORT"

"INTERRUPT STATUS REGISTER VALUE CHECK AFTER READ TERMINATED WITH TARGET ABORT"

"CHECK NORMAL BURST READ AFTER TARGET ABORT TERMINATED BURST READ"

"WB ERROR STATUS REGISTER VALUE AFTER MASTER ABORTED I/O WRITE"

"WB ERRONEOUS ADDRESS AND DATA REGISTERS' VALUES AFTER MASTER ABORTED I/O WRITE"

"INTERRUPT STATUS REGISTER VALUE AFTER MASTER ABORTED I/O WRITE"

"PCI DEVICE STATUS REGISTER VALUE AFTER MASTER ABORTED I/O WRITE"

"MASTER ABORT WHEN ACCESSING TARGET WITH UNSUPPORTED BUS COMMAND - RESERVED2"

"MASTER ABORT WHEN ACCESSING TARGET WITH UNSUPPORTED BUS COMMAND - RESERVED3"

"MASTER ABORT WHEN ACCESSING TARGET WITH UNSUPPORTED BUS COMMAND - DUAL_ADDR_CYC"

Following testcases are for testing fast back-to-back writes and reads through IMAGEs. Task location for testcases is: **run_tests –> target_fast_back_to_back**.

"FAST BACK TO BACK THROUGH TARGET - FILL WRITE FIFO, CHECK RETRY ON FAST B2B WRITE"